REMARKS

Claims 1-5, 8-11, and 13-19 remain pending. Claims 8, 9, 15, and 17 have been amended.

In the Office Action, the Examiner objected to claims 8, 9, 15, and 17; rejected claims 1-5, 8-11, and 13-19 under 35 U.S.C. § 101; rejected claims 14, 15, 18, and 19 under 35 U.S.C. § 102(b) as being anticipated by Shyu (U.S. Patent No. 5,471,412); and rejected claims 1-5, 8-11, 13, 16, and 17 under 35 U.S.C. § 103(a) as being unpatentable over Shyu.

Claims 8, 9, 15, and 17 have been amended to obviate the objections thereto.

§ 101 rejection:

Applicants respectfully traverse the § 101 rejection of claims 1-5, 8-11, and 13-19.

First, with respect to claims 1-5, 8-11, 13, 16, and 17, the rejection as stated was improper and incorrect. These claims recite "a system, comprising: a computation block; a buffer block . . . includ[ing] at least one first buffer . . . and at least one second buffer; and a demultiplexer." Because claims 1-5, 8-11, 13, 16, and 17 are directed to a machine or article of manufacture, they are not "a step of manipulate data for numerical computations" as alleged, and are statutory. See M.P.E.P. § 2106, pg. 2100-15 (and the cases cited therein): "A claim limited to a machine or manufacture, which has a practical application in the technological arts, is statutory. In most cases, a claim to a specific machine or manufacture will have a practical application in the technological arts." These system claims are plainly statutory, and the § 101 rejection of claims 1-5, 8-11, 13, 16, and 17 should be withdrawn.

Second, with respect to claims 14, 15, 18, and 19, these method and system claims recite, among other things, "storing the data value in a multiplication buffer that stores only data values to which a first mathematical operation performed thereto is multiplication; storing the data value in an addition buffer that stores only data values to which a first mathematical operation performed thereto is addition; and outputting a data value stored in the multiplication buffer and an associated data value stored in the addition buffer to a computation block for processing, wherein the determining is performed upstream of the computation block." These claims recite sufficient structure to prevent them from being directed merely to an "abstract idea" (see Interim

Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, OG, 11/22/05. The recitation of an addition buffer, a multiplication buffer, and a computation block distances the claims from pure ideas or algorithms in the abstract. Thus claims 14, 15, 18, and 19 are statutory in accordance with the Interim Guidelines and M.P.E.P. § 2106, and the § 101 rejection of claims 14, 15, 18, and 19 should be withdrawn.

For at least these reasons, Applicants respectfully request withdrawal of the § 101 rejection of claims 1-5, 8-11, and 13-19.

§ 102(b) rejection of claims 14, 15, 18, and 19:

Applicants respectfully traverse the 35 U.S.C. § 102(b) rejection of claims 14, 15, 18, and 19 over Shyu. Claims 14, 15, 18, and 19 require a method including, *inter alia*, "determining whether the data value corresponds to one of an addition operation and a multiplication operation; and outputting a data value stored in the multiplication buffer and an associated data value stored in the addition buffer to a computation block for processing, wherein the determining is performed upstream of the computation block." Shyu fails to disclose all limitations of claims 14, 15, 18, and 19.

Page 4 of the Office Action alleges that the claimed "determining . . ." act is disclosed "from the output port of either 735 or 722 and col. 6, lines 32-43." This cited portion of Shyu, however, only provides (emphasis added):

> The data register unit 4 is a four-port register file, such as a random access memory (RAM) with two write ports (WP1, WP2) and two read ports (RP1, RP2). The first set of read and write ports **(RP1, WP1) of the data register unit 4 are connected to the butterfly operation unit 2**, while the second set of read and write ports **(RP2, WP2) of the same are connected to the multiplication operation unit 3**. The data register unit 4 serves to store data from the butterfly operation unit 2 and the multiplication operation unit 3, and serves to provide data thereto.

This portion of Shyu explicitly teaches that the output of MUX 735 is connected to two dedicated registers RP1/WP1, while the output of butterfly unit 722 is connected to two other dedicated registers RP2/WP2.

Such a hard-connection of two outputs simply does not disclose "determining whether the data value corresponds to one of an addition operation and a multiplication operation" as required by claims 14, 15, 18, and 19. Neither MUX 735, butterfly unit 722, nor data unit 74 performs the claimed determining act. Because Shyu fails to disclose at least the "determining . . ." act, the § 102(b) rejection is improper and should be withdrawn.

Further, page 4 alleges that data unit 83 in Fig. 7 of Shyu discloses the claimed "outputting . . ." act. Data unit 83 does not reasonably disclose the claimed outputting, because the elements that it outputs data to (i.e., MUX 821 and MUX811, presumably considered to correspond to the claimed computation block) are *not* downstream of those elements alleged to correspond to the claimed determining act. In other words, Fig. 7 of Shyu does not structurally disclose "wherein the determining is performed upstream of the computation block," as required by claims 14, 15, 18, and 19.

Nor do MUX 84 in Fig. 7 or MUX 5 in Fig. 4 disclose the claimed outputting, because they only output one or the other of their inputs see col. 6, lines 43-45 (emphasis added):

> The output unit 5 is a multiplexer which selects the output of the butterfly circuit 22 **or** the multiplier circuit 33, **depending on whether** DCT or IDCT is being performed.

These multiplexers in Shyu plainly do not disclose "outputting a data value stored in the multiplication buffer and an associated data value stored in the addition buffer to a computation block," because they can only output one value.

Because Shyu also fails to disclose at least the "outputting . . ." act, the § 102(b) rejection of claims 14, 15, 18, and 19 is improper and should be withdrawn.

§ 103(a) rejection of claims 1-5, 8-11, 13, 16, and 17:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See M.P.E.P. § 2143.

Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection of claims 1-5, 8-11, 13, 16, and 17.

A *prima facie* case of obviousness has not been established for claims 9-11, 13, 16, and 17, because there is no suggestion or motivation to modify Shyu as proposed. Page 6 of the Office Action proposes in essence relocating DE-MUX 71 in Fig. 7 to be immediately in front of 4-Port Data Unit 74 for purposes of sending data "efficiently." The cited portion of Shyu (i.e., col. 5, lines 32-38) only describes the operation of input unit 1 *in its current configuration*. As such, it provides zero motivation to make any changes to the current configuration shown in Figs. 4 and 7 of Shyu. Thus, No facts or other evidence of a suggestion or motivation have been provided in Office Action, and a *prima facie* case of obviousness has not been established.

Nor can a *prima facie* case of obviousness be established, because such a modification of Shyu would necessarily alter the principle of operation of the reference. See M.P.E.P. § 2145(X)(D) ("proposed modification cannot render the prior art unsatisfactory for its intended purpose or change the principle of operation of a reference").

Finally, Applicants note that DE-MUX 71 does not perform the functions of the claimed demultiplexer, because it just operates "in accordance with the intended transform operation" (col. 5, lines 36 and 37). Nor would it be particularly "efficient" as alleged in the Office Action to replace the direct connections to unit 74 (i.e., WP2A and WP1A) in Fig. 7 with a demultiplexer. Both of these additional facts would weigh, in the mind of one of ordinary skill in the art, against the proposed modification of Shyu.

Because no motivation to combine the references has been shown, a *prima facie* case of obviousness has not been established for claims 1-13, 15, and 27-31, and the rejection thereof should be withdrawn.

Reconsideration and allowance of claims 1-5, 8-11, and 13-19 are respectfully requested.

In the event that any outstanding matters remain in this application, Applicants request that the Examiner contact Alan Pedersen-Giles, attorney for Applicants, at the number below to discuss such matters.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0221 and please credit any excess fees to such deposit account.

Respectfully submitted,

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